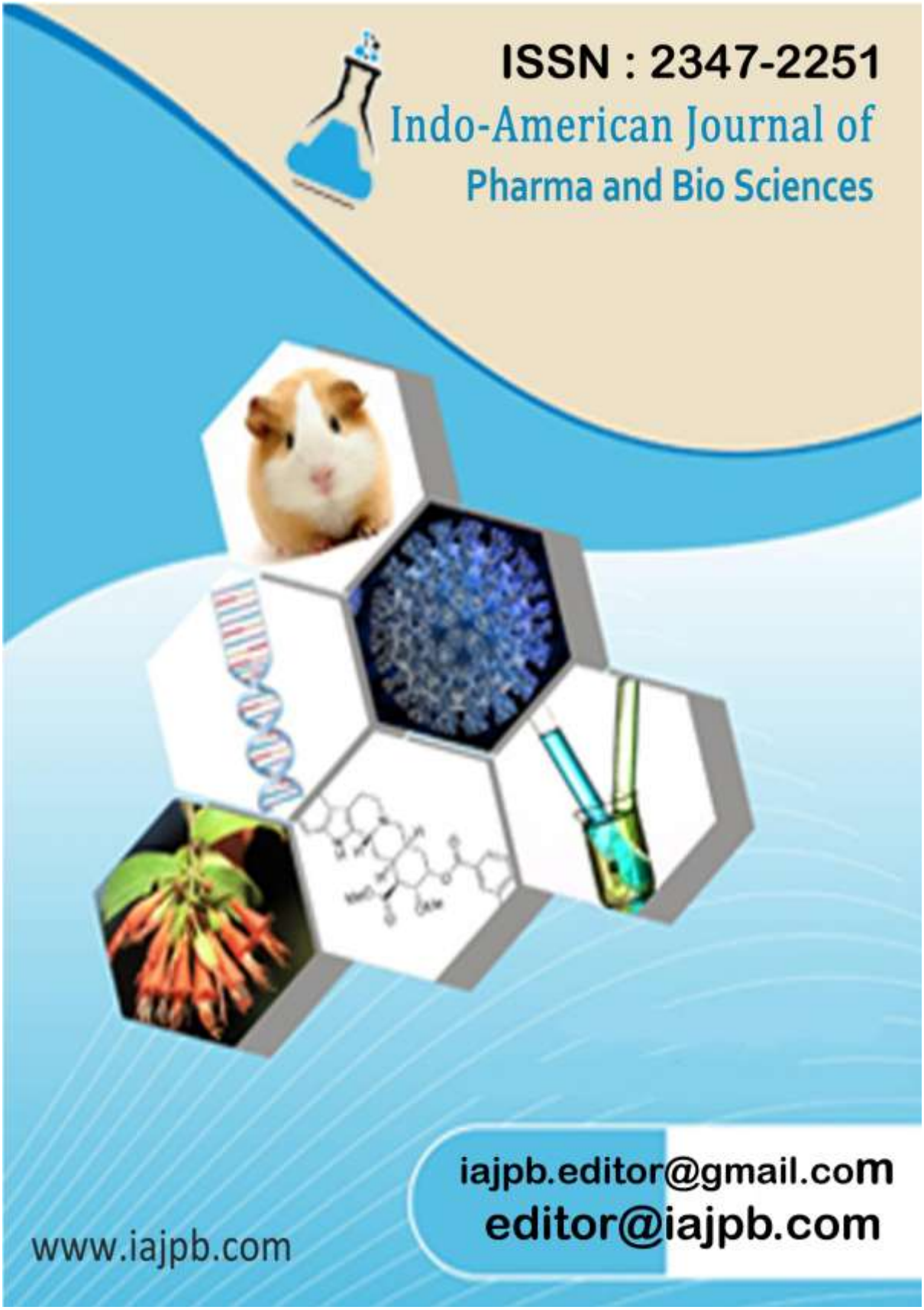
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Efficient Multiple Error Correction by Using Two Bit Overlap Codes

Shaik Mohammad Rafi,M.Sreedhar.

M.Tech Student, DECS (ECE),JNTU College of engineering

Abstract: Error-correction codes are a common way to guard against data corruption. OLS codes frequently make use of linear block codes with single- and double-error correction. Orthogonal Latin square (OLS) codes are a type of one-step majority-logic-decodable (OS-MLD) error correcting codes. Decoding these codes is quick and simple because to the use of short codes. Soft faults in semiconductor memories, OLS codes are used to rectify multiple cell failures. Reconfigurable designs like field programmable gate arrays can benefit from OLS codes generated from Latin squares (FPGA). By adopting Latin Square codes, this work describes the parity regulation matrices and the strategy for lowering the decoding block by enlarging the original OLS code. This work describes the implementation of orthogonal Latin square codes by their parity control matrices and the method of lowering the decoding block by enlarging the real size of the OLS code. The generalization problem is addressed in this study by narrowing the scope of the suggested technique to only include codes with improved errorcorrection.

I.INTRODUCTION

As a result of manufacturing flaws, aging or radiation-induced soft mistakes, electronic circuits in the nanoscales are susceptible to failures. For example, a soft error in a memory might corrupt data and cause a device failure by changing the content of a word. Consequently, error correcting codes are frequently used to secure memory in apps that require reliable operation (ECCs). It is possible to detect and correct errors by adding a certain amount of parity bits to each word. When writing to memory, parity checks are performed, and the results are then read back from memory. To encode and decode, this necessitates additional logic equipment. More parity check bits per word means more errors can be corrected, but more complicated logic circuitry means more errors can be corrected. If the mistake rate is high, memory cells may be affected in an unpredictably random manner. Near-threshold caches, for example, or Spin-transferThe use of torque magneto-resistive RAMs (STT-MRAMs) is necessary for the multiple bit error correction they enable. Some commonly used codes, such as the BCH codes, have a link between the number of parity bits and the number of defects that can be repaired. The decoding difficulty of BCH codes can be significantly increased if a

AnantapurEmailId:s.rafimohammad95@gmail.com
AssistantProfessor(Adhoc),Dept.ofECE,JNTUCollegeofengineeringAnantapurEmailId:sreedhar470@gmail.com

Correction Codes and poses a limiting design constraint, even though decoding is possible.
In addition to Euclidean Geometry, Difference Set codes, and codes for Orthogonal Latin Square, codes for memory protection have been investigated extensively during the previous millennium; codes besides Euclidean Geometry, Difference Set codes, and codes for Orthogonal Latin Square have been configured. Fast decoding is possible in all of these circumstances thanks to Another Step Majority Logic Decoding. With a handful of \Two-bit error correction codes (i.e. Double Error Correction (DEC)) and word sizes more than 10 bits are the only viable design alternatives afforded by OLS codes.
These codes use a lot of parity check bits, which means they take up a lot of memory space.
As a result, discovering new code installs that encourage OS-MLD as successful and creative design solutions has a great deal of promise. Double Error Correction codes supporting OS-MLD are described in this research using a novel technique. The new structure is based on the employment of parity control matrices with constant weight and just one or two points of intersection. OS-MLD, which is substantially more difficult to design than Orthogonal Latin, can now be improved.
The decoding of Square codes, however, is a little better than that of non-OS-MLD codes, such as BCH codes.OLS codes, which are also used to safeguard memory, were implemented generations before the proposal to protect interconnect and cache. k = m two data bits and two tm parity bits make up the block dimensions of Orthogonal Latin Square codes. An integer m is substituted for t, denoting the number of errors that have been fixed. For memory, word dimensions are frequently a power of two, as is m. One of the main advantages of OLS code is that it is simple and affordable to decipher. Because of this, OS-MLD can be used to decode OLS codes. When it comes to DS codes and OLS codes, what is the situation? Orthogonal Latin Square codes appear to be based on the idea that: 1) every data bit is involved in perfectly 2t parity control bits; 2) every other data bit is involved through at most those parity control bits.

equation parity checks, OS-MLD decodes each bit. Compared to syndrome decoding, where each bit is compared to the applicable error patterns and many syndrome patterns must be taken into account when multiple bits need to be rectified, the entire system is much simpler. Most OS-MLD code difficulties stem from the fact that it is only supported by a small number of codes, each having a limited number of word sizes and error correcting features.

In the Double Error Correction Orthogonal Latin Squarecodes, the proposed and removed SEC-DED-DAEC codes (DEC-OLS codes). A parity check matrix is used as the starting point for the first step, which is to remove the m parity check bits corresponding to one of Mi. For each equation in the reduced matrix, each transmitting data bit will indicate a parity check that has been deleted. Furthermore, these m-bit groups are referred to as g1, g2, g3, and g4 in Fig. When M1 is eliminated, there is no change in the parity check bit. G2 and G3 and G4 refer to the groupings of bits 9-12 and 13-16 correspondingly. Three parity checks are performed on the updated matrix, and each bit of data is included in each check. As a result, single-bit and double-bit errors can be fixed using a majority vote decoding algorithm.

II. EXISTINGMETHOD

The limitations of these codes are also used to assess and establish Two Bit Overlap (TBO) codes. The matrices used to create the codes are examined in the first section, which demonstrates how they can be utilized to generate DEC OS-MLD codes. Sub-section two introduces the procedure for putting together matrices, while sub-section three details the parameters of proposed codes.

MatrixFeatures

Building OS-MLD codes using the preceding section's Double Error Correction (DEC) approach necessitates the creation of column matrices such that:
2. Each column has four rows.

Only one column in a pair of columns shares a position with another column.Orthogonal Latin Squares with double error correction is an example of this type of architecture.

Because each column corresponds to a data bit and each row corresponds to a parity check bit, the entire matrix can be utilized for parity checks in which the columns correspond to the data bits, and each row corresponds to a parity check bit.

Orthogonal Square-Majority Logic Decodable property is easy to understand because each input data is parity checked four times, while the other bits represent this at only one parity check.

There is still a problem, because two parity checks on the initial bit will produce faults on the other bits, therefore an error cannot be made.

This will be the code for DEC if at least five of the seven equations for the participating bit have a majority. There are a number of possible outcomes, including the following:

First, there is no plurality and no incorrectly since the error free bit has a worst case of four parity check faults. A bit in error and another bit in error are to blame for at least five parity check faults on the incorrect bit, thus it will be fixed.

In terms of decoding and encoding, this code is more complicated than a DEC OLS code. It's because of these two things:

It takes more reasoning to measure parity tests since there are more matrices in the matrix (seven instead of four per column).

The majority vote is carried out using seven parity tests and not more than four, which is yet more complicated.

However as detailed in the evaluation section of this paper,the decoding is still significantly simpler than for a non OS-MLD language. The proposed codes need to have a lowernumberofparitycheckbitstohaveanadvantageovercurrent DEC OLS codes. As seen next, this will be the caseforthe suggestedscheme.

PolynomialbasedMatrix Construction

To create matrices with the attributes listed in this section, take these steps. Each bit with index b is associated with a polynomial P of degree two, so that b is associated with P.

Code word data bits are encoded as [0,3k-1] for each of its three coefficients.Thecoefficients.

Considerabuildinginwhichthematricesaregiven insucha

areselectedsuchthatPb(x)=∑2 $ai.xi$satisfiesPb(3√k)= waythat: ai.(3√k)i=b.Notethatthereisasingleoptionforthe

1. Thereareexactly7columnseach.2.With onein particular,eachpairofcolumnshasjusttwopositionsatmost.

selectionofa,a,a.Forinstance,aequalsbmod 3√k,a1=((b−a0)/3√k)mode3√$k$and$a$2=((b−a0−a1.3√k)/(3√k

Then the coefficients of the polynomial are$a$0= 51mod7=2;a=51−2mod7= 70$and$$a$2(51−2−0.7)$mod$7=1so that P(x)=2+x2

polynomialwithdegree2,hasthreerootsthatare notpossibleasperLagrangestheorem.eThismeans,therefore

thatPbiscompletelyquavalenttoPc.

consequently,B=c

whichsatisfies$P$51(3√k)=P51(7)=2+72=51.

We next use the seven polynomial values to describe each b bit so that modulo3k calculations can be performed. Such values will be bb = 51: bb = 2, 3, 6, 4, 4, 6, 3 There is a representation for each of these values3k. An arrangement of bits where each bit represents an integer, while the rest are zeros, resulting in a value of one. As with the ordered sequence of values, a binary vector length describes it.

and the two bits are same which eliminates the hypothesisthatthese bitswere different.

Thebuildingjustmentionedwouldthereforeproducematrices with columns which have exactly seven columnsand that share two at most. Let us summarize the mechanismofconstruction:

1. Choose a block size k such that 3√$k$is a prime more thansix.2. For every position ofkbits allocate an index b = 0, 1,2…k-1.3.ComputethepolynomialPb(x)=

3√k.

∑2.xiwhichsatisfies$P$(3√k)=bwithcoefficientsthat

i=0 b

That list would be {0010000, belongto

the column of the data bit b and has exactly seven (satisfyingthefirstcondition). 3k37k.

There are two additional conditions met when a prime number is higher than or equal to seven, as mentioned in the previous subsection. At most, two columns are allowed in each matrix column, according to this rule. On the basis of Lagranges' theorem, which stipulates that a polynomial of degree n>1 modulo, a prime number P with integer coefficients that are not divisible by P, may only have one root at most.

There are no coefficients modulo that are divisible by and over which they are also smaller than for the polynomials employed in the code building. Assume, for the sake of argument, that the parity check matrix's bits b and c each contain three bits or more. These two polynomials, Pb(x) and Pc(x), show at least three distinct values overlapping, each with a degree of 2. Thereby suggesting that the product of lead and tin is a obtained in 4 such that the bit thatcorresponds to the valueis 1 and all the other bits are 0. 6. The column of the paritycheck matrix for that bit is formed by the concatenation ofthesevenarraysobtainedin step5.

For such a specified prime number p, the codes acquired getthe following parameters: and n-k=7. P. Which comparescorrelates to codes which have OLS & when p is big, n-k=4.p.TBOCodes

ThespecificationsoftheTBOcodesacquiredwith thepolynomialconfigurationwassummarized.ThespecificationsoftheDECOLScodeswithsimilar wordlengths are also seen in this table; just a few word sizesbeginning at k = 343 are supported. This could be used byshorteningitsHmatrixforthesecurityof256bit words.Single parity bit can be preserved after extracting 87columnsthatoccupy most1positions fromH matrixof each

[0,3√k−1].4.Computethe valuesofthepolynomial3√$k$for

0001000,0000001,0000100,0000100,0000001,0001000}in

3√$k$bitarraytoeachofthevalues

ourexample.Intheparitysearchmatrix,thisvectorwillbe

So the proposed code requires 48 parity check bits similar to 64 for a DEC OLS code. Security may be ensured for 1024-bit words with the following block size, k = 1331 (as applicable to some con-figurations for cache memory). In this scenario, the suggested code could be simplified and permits 75 parity bits in comparison to 128 for DEC OLS code by maintaining 2 parity bits.

III. PROPOSEDMETHOD

In communication, data is often received sequentially and decoded bit-by-bit. Decoding is made tough by the requirement to decode a complete word in one go. SEC (Single Error Correction) codes are commonly employed to preserve memories. Decoding is possible for each bit in such a circumstance by comparing the syndrome to the corresponding column in the parity check matrix.

However, if more than one bit needs to be fixed, such as

1. The size of each column. 7. k 2. Every column referring toabitofdatahasexactlysevencolumns.3.Everysetofcolumns only has two positions as a maximum, with one indefault(twobitoverlap).

ConstructionoftheParity CheckMatrix:

There are orthogonal Latin Square codes that are taken from Latin squares. If the set 0, 1, 2...m-1 is used, then each row and column in the Latin square will only contain one instance of each element, which is known as an array of Latin squares with size m*m. It is not possible to derive an OLS code from the Latin squares of dimension m for secure data with k-bits of length from the OLS code. The OLS code adjustment t-error has 2 parity bits.

an approach called as syndrome decoding, wants to evaluatethe various bit error syndromes that contain the bit.

Whichleadstoasignificantincreaseinthecomplexitiesof decoding,particularlyforlargewordsizes.OneStepMajorityLogicDecodable(OS-MLD)codeshavebeendevelopedtosecurememoriesinordertoaddressthelimitationsofsyndrome-baseddecoding.Formemorysecurity, some OS-MLD codes, such as the Orthogonal LatinSquare codes, was suggested decades ago. In certain cases,however,theyrequirealargenumberofbitsforparitytesting. The number of parity check bits is minimized bythese codes. The maindifficult with EG as well as DS codesis that merely a few block sizes as well as error correctionfunctionalityaresupported.Forinstance,EGcodesonlysupport(n,k)forDoubleErrorCorrection(DEC),thatcorresponds to a code word size n as well as the data blocksizek.

Double error correction Orthogonal Latin Square codes aredesignedtohavefollowingcharacteristicsfortheparitycheck matricesH: M1 and M2 are both identity matrices of size m x m, and the number of 1s in each row is equal to m. There are a number of sub-matrices produced from pairwise orthogonal Latin squares, i.e. M3, M4,... M2t.

A basic decoding scheme can be devised based on these characteristics. The seven parity check equations involved in this system are used to perform a majority vote on each piece of data. If the answer is one, the bit has been found to be incorrect and will be fixed. Decoding this way is known as one-step majority logic.Data bits will be corrected even if there are single and double mistakes. The other two bits can only effect two of its parity tests if the bit itself is correct, therefore there is no majority to begin a correction if the bit is accurate.

Data bits are represented by the left n2 * n2 columns in the parity check matrix H for Double Error Correction Orthogonal Latin

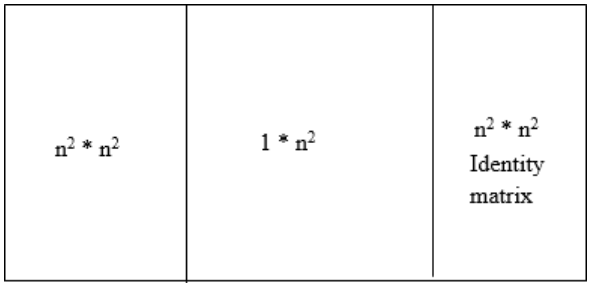


Figure 1: Parity check matrix H of the (n, 1, k) DEC OLScode.

Square coding, which can be seen in Figure 1. In order to verify all potential two-bit error patterns for a bit, the required logic circuit is easier than testing all of them. Because the number of possible double bit error patterns is directly proportional to n, this feature is more useful when the code word size is big.Each row of an OLS code contains equations for the code word calculation, and these equations can be directly sent into XOR gates such that the parity bits can be created by XORing each row's bits. Hence, in the Orthogonal Latin Square codes parity check matrix, there are equal numbers of parity bits and rows. In the decoder of an OLS code with a size of 1*n2 depicted in the picture, one-step majority logic decoding takes place.n has to be a prime number, which we figured out as 7 in this design. Each decoding bit is 1*49 of an identity matrix that is 49x49. Parity check equations are recomputed with the bit to produce each code word bit, and then a majority vote is conducted among the parity check equations. It is only if an error has occurred that the value of the resultant parity check equation or the syndrome bit changes from 0 to 1.

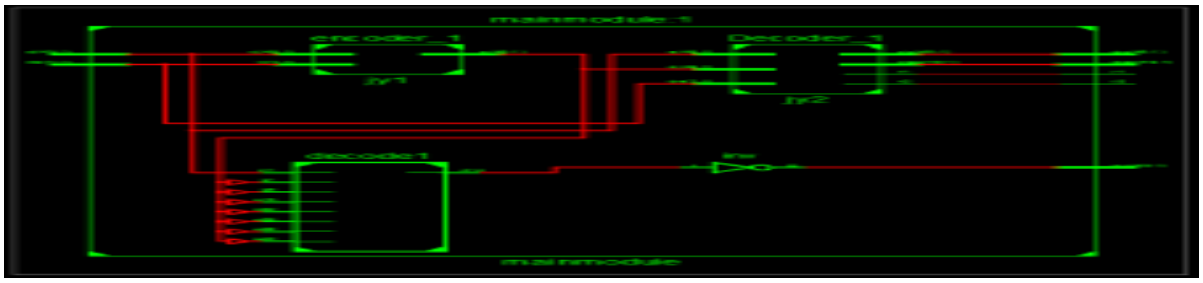
If the majority of the syndrome bits turn into 1, then it isevident that an error has altered the state of the bit, and so,the bit necessities to be corrected. The re-computing of theparity check bits is done by modulo-2 adders or XOR gateshaving suitable number of inputs. By using a 2-input XORgate the error can be corrected at the end of themajoritylogic circuit, where one of the

inputs is the bit itself and theother oneistheoutputofthemajoritylogiccircuit.

RESULTS ANDDISCUSSION

Orthogonal Latin square codes are quite effective when it comes to correcting errors involving many bits. Encoding and decoding of the OLS codes for huge data blocks is now possible thanks to this research. Compared to the current method, the area and the latency will be reduced in the proposed method.

RTLSchematic



Simulationresults:

TechnologySchematic

CONCLUSION

As compared to other existing multi-bit error correcting codes, orthogonal Latin square codes are highly efficient in correcting multi-bit errors without sacrificing substantial area, and the encoders and decoders can be implemented in comparatively simple circuits. Encoding and decoding of the OLS codes is possible for larger data blocks and a wide range of lengths thanks to their great modularity and flexibility. Implementation on an FPGA platform has shown that the encoder and decoder are both simple and fast.

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